SEMICONDUCTOR DEVICE HAVING A GATE AND FABRICATION METHOD THEREFOR

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to a semiconductor device having a gate and a fabrication method therefor which improve thermal stability, lower resistance and simply fabrication.

Background of the Related Art

[0002] A related art method for forming a gate electrode in a semiconductor device will be explained with reference to the attached drawings. Figs. 1A ~ 1C are sectional views of a semiconductor device during fabrication, which figures illustrate the steps of a related art method for forming a gate electrode. The high gate resistance caused by miniturization of the semiconductor device decreases the device operation speed. Consequently, a gate electrode with a low resistance is required. To meet such a requirement, a refractory metal silicide having a low resistance is employed for the gate electrode. This refractory metal silicide is called a polycide (silicide on doped polycrystalline-Si). Of the polycides, WSi_2 (resistivity 60 ~ 200 μΩ/cm) is the most widely used. However, a polycide having a resistance lower than that of the WSi_2 is $CoSi_2$ (resistivity 15 ~ 20 μΩ /cm) and $TiSi_2$ (resistivity 15 ~ 20 μΩ /cm).

[0003] First, a thermal process conducted after formation of a silicide agglomerates the silicide, with an increased resistance. $CoSi_2$ shows an excellent thermal stability with less agglomeration than $TiSi_2$.(J. B. Lasky et al. IEEE Trans. Elec. Dev., 38, 262(1991), L. Vanden hove, VLSI tecnol., (1987). P.67).

[0004] Referring to Fig. 1A, in the method for forming a gate electrode of such a refractory metal, a gate oxide film 2 is formed on the semiconductor substrate 1. A polysilicon layer 3, a silicide layer 4, and an insulating layer 5 are then stacked on the gate oxide film 2 in succession, insulating layer 5 being used as a hard mask. As shown in Fig. 1B, the insulating layer 5 is subjected to patterning by photolithography, and the silicide layer 4 and the polysilicon layer 3 are subjected to selective patterning by a dry etching process using the patterned insulating layer 5 as a mask, thereby forming a gate electrode layer 6. As shown in Fig. 1C, an insulating layer for forming gate sidewalls is deposited on an entire surface including the gate electrode layer 6. The insulating layer is etched back to form sidewalls 7 located only at the sides of the gate electrode layer 6. In this instance, the refractory metal is Co or Ti.

[0005] Of $CoSi_2$ and $TiSi_2$, which have similar resistivities, $CoSi_2$ has conventionally been preferred for formation of the gate electrode for at least the following reasons.

[0006] First, a thermal process conducted after formation of a silicide agglomerates the silicide, with an increased resistance. $CoSi_2$ shows an excellent thermal stability with a less agglomeration than $TiSi_2$.(J. B. Lasky et al. IEEE Trans.

[0007] Elec. Dev., 38, 262(1991), L. Vanden hove, VLSI tecnol., (1987). P.67).

[0008] Second, in comparison to a sharp increase in resistance in the case of $TiSi_2$ when the width of the gate line is reduced, the resistance of $CoSi_2$ is kept low even if the gate line width is reduced.

[0009] Third, $CoSi_2$ may be used as SADS(Silicide as A Dopant Source) for easy doping of polysilicon. SADS is a method for doping a silicon layer by heating, and diffusing dopant injected in a silicide into an underlying silicon layer. Though $CoSi_2$ can be used as SADS, $TiSi_2$ can not be used as SADS, because $TiSi_2$ has a high reactivity with dopants like As, P, and B.(K. Maex et al., J. Appl. Phys., 66, 5327(1989), V. Probst et al., J. Appl. Phys., 52, 1803(1988), F. C. Shone et al., Int. Elec. Dev. Meet., (1986), p. 407).

[0010] Because of the properties of $CoSi_2$, attempts have been made to form the gate electrode of $CoSi_2$.

[0011] However, despite of its advantage of low resistance, the related art method for forming a gate electrode of a refractory metal silicide has at least the following problems related to etching. $CoSi_2$ is difficult to etch, causing problems in patterning a gate line.(F. Fracassi et al., J. Electrochem. Soc., 143. 701(1996)). Though etching by converting into TiF or TiCl2, which are volatile, is widely used in the case of $TiSi_2$ in a dry etching(T. P. Chow et al., in Dry Etching for Microelectronics, R. A. Powell, Editor, p. 40, Elsevier Science, New York(1984)), as cobalt is very stable without any volatile chemical compounds, etching of cobalt is very difficult.(A. E. Morgan et al., J. Electrochem. Soc., 134, 925(1987)).

SUMMARY OF THE INVENTION

[0012] The present invention is directed to a semiconductor device having a gate and a fabrication method therefor that substantially obviate one or more of the problems due to limitations and disadvantages of the related art.

[0013] An object of the present invention is to provide a semiconductor device having a gate and fabrication method therefor, which result in improved thermal stability, low resistance, and simplified fabrication.

[0014] Additional features and advantages of the invention will be set forth in the description which follows, and in part will be apparent from the description, or may be learned by practice of the invention. The objectives and other advantages of the invention will be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0015] To achieve these and other advantages and in accordance with the purpose of the present invention, as embodied and broadly described, the method for forming a gate in a semiconductor device, for improving a thermal stability, providing a low resistance, and assuring an easy fabrication process, may include (1) forming a first insulating film and a conductive film on a semiconductor substrate, (2) patterning the first insulating film and the conductive film, to form a gate, (3) forming a second insulating film thicker than the gate on an entire surface, (4) planarizing the second insulating film, to expose the gate, (5) depositing a refractory metal layer on an entire surface, (6) forming a silicide layer on an upper surface of the gate by heat treatment, and (7) etching the refractory metal layer and the second insulating film.

[0016] It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description serve to explain the principles of the invention. In the drawings:

[0018] Figs. 1A ~ 1C illustrate sectional views of a semiconductor device showing steps of a related art method for forming a gate electrode; and,

[0019] Figs. 2A ~ 2G illustrate sectional views of a semiconductor device showing steps of a method for forming a gate electrode in accordance with a preferred embodiment of the present invention, Fig. 2G showing the completed semiconductor device having the gate electrode formed in accordance with the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0020] Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings. Figs. 2A ~ 2G illustrate sectional views of a semiconductor device showing steps of a method for forming a gate electrode in accordance with a preferred embodiment of the present invention. The present invention assures an easy fabrication process in forming a $CoSi_2$ gate electrode which has a good thermal stability and a low resistance.

[0021] Referring to Fig. 2A, the method for forming a gate electrode in accordance with a preferred embodiment of the present invention starts with forming a gate oxide film 22 on a semiconductor substrate 21, and forming a material layer 23 for forming a gate, for example, a conductive film, such as a polysilicon layer, to a thickness of 2500A (±5%). As shown in Fig. 2B, material layer 23 is selectively patterned to form a material pattern layer 23a for forming a gate. Then, as shown in Fig. 2C, an insulating layer 24, for example, an oxide film or a nitride film, is formed to a thickness of 2500 ~ 3500A on an entire surface including the material pattern layer 23a for forming a gate. As shown in Fig. 2D, the insulating layer 24 is planarized by CMP (Chemical Mechanical Polishing), to expose a top surface of the material pattern layer 23a for forming a gate, (the planarized insulating layer is identified as 24a). Then, as shown in Fig. 2E, a refractory metal layer 25, for example, a Co layer, is formed to a thickness of 300A (±5%) on the planarized insulating layer 24a and the material pattern layer 23a for forming a gate. And, as shown in Fig. 2F, a silicide layer 26, for example, a $CoSi_2$ layer, is formed by a thermal treatment process at an interface of the refractory metal layer 25 and the material pattern layer 23a for forming a gate. As shown in Fig. 2G, after silicide layer 26 has been formed, the portion of refractory metal layer 25 that [made no reaction] has not reacted due to the planarized insulating layer 24a is wet etched. To wet etch the refractory metal layer 25, a H_2SO_4 or HCl-based solution is used. Then, as also shown in Fig. 2G, the planarized insulating layer 24a is removed. An insulating film is thereafter again deposited on an entire surface and etched back to leave insulating film at sides of the gate electrode, thereby forming gate sidewalls 27. In this instance, the gate electrode has a total thickness of approximately 2000A (±5%), with a polysilicon layer of a 1000A (±5%) thickness, excluding a loss portion during the silicide reaction and the silicide layer thickness of approximately 1000A (±5%).

[0022] Thus, the method for forming a gate electrode of $CoSi_2$ in the present invention allows formation of the gate electrode without a separate silicide layer patterning process, by patterning a polysilicon layer, which is a lower layer of the gate electrode, before making a silicide reaction only on the patterned polysilicon layer.

[0023] The method for forming a gate electrode of $CoSi_2$ using the concepts the present invention has at least the following advantages.

[0024] First, $CoSi_2$ can be used as a polycide despite its poor etchability. That is, the method for forming a gate electrode of $CoSi_2$ of the present invention allows formation of the gate electrode without a separate silicide layer patterning process, by patterning a polysilicon layer that is positioned as a lower layer of the gate electrode before a silicide reaction occurs, thereby limiting the silicide reaction to the patterned polysilicon layer and assuring an easy fabrication process.

[0025] Second, because no separate silicide layer patterning is performed, no etching damage is experienced, eliminating the need for an oxidation process ordinarily required for recovering the damage to the gate oxide film. Because the silicide is not oxidized in this manner, a loss of Si can be prevented.

[0026] Third, the formation of the silicide, not in source/drain regions, but only in the gate electrode layer, solves the problem of junction leakage in the source/drain regions.

[0027] It will be apparent to those skilled in the art that various modifications and variations can be made in the method for forming a gate in a semiconductor device of the present invention without departing from the spirit or scope of the invention. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.